

5 a sense amplifier for sensing the position of the measurement mass within the sensor.

1 ~~31~~ 31/4. The apparatus of claim 1, wherein the controller further comprises:
2 a loop filter for providing control to the sensor apparatus, to the loop filter including:
3 one or more integrators for providing a signal for controlling the sensor system;
4 one or more derivative controllers for providing a signal for controlling the sensor
5 system;
6 one or more proportional controllers for providing a signal for controlling the sensor
7 system; and
8 a summer for combining the signals from the integrators, the derivative controllers, and
9 the proportional controllers.

1 ~~32~~ 32/5. The apparatus of claim 1 further comprising:
2 a multiphase clock generator for providing clock signals for controlling the operation of
3 the apparatus, the clock generator including:
4 a digital signal generator; and
5 a data-independent clock resynchronization circuit coupled to the digital signal generator
6 for resampling clock signals.

1 ~~33~~ 33/6. The apparatus of claim 1 further comprising:
2 a sensor simulator for simulating the operation of a sensor, the simulator including;
3 a filter adapted to receive one or more input signals and generate an output signal
4 representative of the operating state of the sensor; and
5 an input signal selector operably coupled to the filter adapted to controllably select the
6 input signals as a function of the simulated operating state of the sensor.

1 ~~34~~ 34/7. The apparatus of claim 1 further comprising:
2 a device for testing the operation of the controller, the device comprising;
3 a sensor simulator for simulating the operation of a sensor; and
4 a second controller coupled to the simulator.

1 ~~35~~ 35/8. The apparatus of claim 1, wherein the controller further comprises:
2 a feedback control system for providing control to the apparatus, the feedback control
3 system comprising:
4 a startup sequencer for selecting the mode of operation of the feedback control system;
5 and
6 a loop filter coupled to the startup sequencer.

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1 36. The apparatus of claim 35, wherein the clock resynchronization circuit comprises:
2 a plurality of inverters;
3 a plurality of NOR gates coupled to the inverters;
4 a plurality of NAND gates coupled to the inverters;
5 a plurality of XNOR gates coupled to the NAND gates and the inverters;
6 a plurality of asynchronous set double-edge flip-flops coupled to the NOR gates; and
7 a plurality of asynchronous reset double-edge flip-flops coupled to the NOR gates.

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1 37. A method of controlling the operation of a sensor assembly, comprising:
2 using a controller to apply electrostatic forces to a sensor to create one or more sensor
3 operating states; and
4 sequentially arranging the operating states into which the sensor is placed to create a
5 plurality of operating modes for the sensor assembly.

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1 38. The method of claim 37 further comprising:
2 determining an operating mode of the sensor assembly;
3 adjusting a mode of operation of a loop filter in the sensor assembly;
4 providing feedback loop compensation to the sensor assembly during a start-up mode
5 of operation for the sensor assembly; and
6 providing noise shaping to the sensor assembly during a sigma-delta mode of operation
7 for the sensor assembly.

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1 39. The method of claim 37, wherein the sensor assembly includes a loop filter, one or more
2 integrators, a proportional controller, the method further comprising:
3 placing a loop filter including one or more integrators, a proportional controller, and a
4 derivative controller in a reduced-order operating mode;
5 sending a signal to the loop filter to control the operating mode of the loop filter; and
6 holding the integrators within the loop filter in a reset mode to place the loop filter in the
7 reduced-order operating mode.

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1 40. The method of claim 39 further comprising:
2 taking the integrators out of the reset mode to place the loop filter in a normal operating
3 mode when the sensor system is operating in a sigma-delta operating mode.

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1 41. The method of claim 39, wherein the operating mode of the loop filter further comprises:
2 sending a signal to the loop filter indicating an operating mode of the sensor assembly;
3 operating the loop filter in a reduced-order mode while the sensor assembly is operating
4 in a start-up mode;

5 operating the loop filter in the reduced-order mode for a predetermined period of time
6 after the sensor assembly transitions from the start-up operating mode to a sigma-delta
7 operating mode; and
8 operating the loop filter in a normal mode during the sigma-delta operating mode after
9 the predetermined period of time during which the loop filter operates in reduced-order mode.

1 ⁴²15. The method of claim ⁴¹14, wherein the operating mode of the loop filter further comprises:
2 operating the loop filter in a reduced-order mode while the sensor assembly is operating
3 in the sigma-delta operating mode.

1 ⁴³16. The method of claim ³⁷10 further comprising:
2 generating a clock signal for the sensor assembly, the generating including:
3 generating a first clock signal; and
4 resampling the first clock signal to generate a second clock signal to restore signal
5 integrity and providing a timing relationship.

1 ⁴⁴17. The method of claim ³⁷10 further comprising:
2 resampling an input signal to the sensor assembly, the resampling including:
3 resampling the input signal in a first level-sensitive latch, including one or more
4 transmission gates, one or more NOR gates, and one or more inverters, on one edge of a clock
5 input signal; and
6 resampling the input signal in a second level-sensitive latch, including one or more
7 transmission gates, one or more NOR gates, and one or more inverters, acting in parallel with
8 the first level-sensitive latch, on another edge of the clock input signal.

1 ⁴⁵18. The method of claim ³⁷10 further comprising:
2 resampling an input signal to the sensor assembly, the resampling including:
3 resampling the input signal in a first level-sensitive latch, including one or more
4 transmission gates, one or more NAND gates, and one or more inverters, on one edge of a
5 clock input signal; and
6 resampling the input signal in a second level-sensitive latch, including one or more
7 transmission gates, one or more NAND gates, and one or more inverters, acting in parallel with
8 the first level-sensitive latch, on another edge of the clock input signal.

1 ⁴⁶19. The method of claim ³⁷10, wherein the controller includes an analog control circuit, the
2 method further comprising:
3 operating the analog control circuit by generating a first clock signal;
4 resampling the first clock signal to generate a second clock signal to restore signal

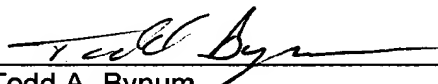
5 integrity and provide a proper timing relationship; and
6 driving the analog control circuit using the second clock signal.

1 ⁴⁷20. The method of claim ³⁷10 further comprising testing the controller, wherein the test
2 comprises:
3 connecting a sensor simulator to the controller;
4 supplying an input signal of a known value to the sensor simulator;
5 converting the input data to the sensor simulator into an output stream from the sensor
6 simulator;
7 sending the output stream from the sensor simulator to the controller;
8 processing the output stream from the sensor simulator within the controller to create
9 an output stream from the controller; and
10 analyzing the output from the controller to determine the accuracy of the controller.

1 ⁴⁸21. The method of claim ³⁷10 further comprising:
2 offsetting the effects of external acceleration forces on the sensor assembly
3 independent of sensor assembly orientation by applying electrostatic forces to a sensor element
4 to offset the effects of the acceleration force.

Respectfully submitted,

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